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Mentor Graphics Customers Expand Use of Calibre Pattern Matching to Tackle Toughest IC Verification and Manufacturing Problems

WILSONVILLE, Ore., June 1, 2016—Mentor Graphics Corporation (NASDAQ: MENT) today announced that customers and ecosystem partners are expanding their use of Calibre Pattern Matching solution to overcome previously intractable IC verification and manufacturing problems. The solution is integrated into the Mentor® Calibre nmPlatform solution, creating a synergy that drives these new applications at IC design companies and foundries, across multiple process nodes.

Calibre Pattern Matching technology supplements multi-operational text-based design rules with an automated visual geometry capture and compare process. This visual approach is both very powerful in its ability to capture complex pattern relationships, and to work within mixed tool flows, making it much easier for Mentor customers to create new applications to solve difficult problems. Because it is integrated into the Calibre nmPlatform toolset, the Calibre Pattern Matching functionality can leverage the industry-leading performance and accuracy of all Calibre tools and flows to create new opportunities for design-rule checking (DRC), reliability checking, DFM, yield enhancement, and failure analysis.

“Our customers count on eSilicon’s design services, IP, and ecosystem management to help them succeed in delivering market-leading ICs,” said Deepak Sabharwal, general manager, IP products & services at eSilicon. “We use Calibre Pattern Matching to create and apply a Calibre-based yield-detractor design kit that helps identify and eliminate design patterns that impact production ramp-up time.”

Since its introduction, use models for Calibre Pattern Matching technology have rapidly expanded, solving problems that were previously too complex or time-consuming to be

implemented. New use cases include the following:

- Physical verification of IC designs with curved structures—for analog, high-power, radio frequency (RF) and microelectromechanical (MEMS) circuitry—is extremely difficult with products designed to work with rectilinear design data. Calibre customers are automating that verification using a combination of Calibre Pattern Matching technology and other Calibre tools for much greater efficiency and accuracy, especially when compared to manual techniques.

- Calibre Pattern Matching technology can be used to quickly locate and remove design patterns that are known or suspected of being difficult to manufacture ("yield detractors"). Foundries or design companies create libraries of yield detractor patterns that are specific to a process node or a particular design methodology. Samsung Foundry used this approach in its Closed-Loop DFM solution to help its customers ramp to volume faster, and reduce process-design variability.

- Some customers use Calibre Pattern Matching technology with Calibre Auto-Waivers™ functionality to define a specific context for waiving a DRC violation. This enhancement allows for automatic filtering of those violations for significant time savings and improved design quality.

"To help our customers create manufacturing-ready designs, we use Calibre Pattern Matching to create and use a yield detractor database to fix most of the litho hotspots in the block level. Then we perform fast signoff DFM litho checking at the chip level using an integrated solution with Calibre Pattern Matching and Calibre LFD" said Min-Hwa Chi, senior vice president, SMIC. "By offering a solution for manufacturability robustness that is built on the Calibre platform, we are seeing ready customer adoption of SMIC's DFM solution."

With the Calibre Pattern Matching tool, design companies can now optimize their physical verification checking to their unique design styles. The tool is easy to adopt because it doesn't rely on expertise in scripting languages. Instead, any engineer can readily define a visual pattern that captures the designer's expertise in the critical geometries and context for that configuration. "With the growing adoption of Calibre Pattern Matching technology, Mentor continues to help our customers address increasing design complexity, regardless of the process node they are targeting," said Joe Sawicki, vice president and general manager of the Design-to-Silicon division at Mentor Graphics. "By incorporating the Calibre Pattern Matching

tool, the Calibre platform becomes an even more valuable bridge between design and manufacturing for the ecosystem."

At the 2016 Design Automation Conference, Mentor has a Calibre Pattern Matching presentation on Tuesday, June 7 at 3PM in the Mentor booth #949. Register for the session ttps://www.mentor.com/events/design-automation-conference/sch h using the registration form edule

Samsung Foundry Closed-Loop DFM Solution Leverages Mentor Graphics Tools to Accelerate Customer Yield Ramps

WILSONVILLE, Ore., June 1, 2016—Mentor Graphics Corp. (NASDAQ: MENT) today announced that Samsung Foundry's Closed-Loop DFM solution uses production Mentor Calibre and Tessent platforms to accelerate customer yield ramps. A successful yield ramp directly impacts customer product cost and time-to-market. In the Closed-Loop DFM flows, Samsung integrates its comprehensive DFM kits with its testing and manufacturing expertise to identify integrated circuit (IC) design patterns that are most likely to impact manufacturing yield, thereby helping customers improve design quality, yield, and ramp to production. The Samsung solution extracts customer yield-averse design patterns, feeds that information forward to optimize manufacturing and testing, and closes the loop with feedback from silicon results for product design and yield improvement. This solution is not only useful to initial customer designs, but it also allows learnings from current production designs to be applied to next-generation designs from that same customer across entire product families.

"Samsung is committed to helping our customers to ramp up as quickly as possible and get to market faster with their semiconductor designs," said JaeHong Park, senior vice president,

Design Services, Samsung Foundry. “Our Closed-Loop DFM solution, which is built on top of Mentor platforms, gives our customers deeper, faster insight into design hotspots, improving quality and yield. Our work has shown more than 10 percent product yield gains in the initial phase of production when compared to the same design without our Closed-Loop DFM system applied.”

“This new use model for the Calibre and Tessent platforms is another milestone in our continued partnership with Samsung,” said Joe Sawicki, vice president and general manager of the Design-to-Silicon division at Mentor Graphics. “Our joint customers can use Closed-Loop DFM with production Calibre and Tessent software to deliver leading-edge products faster on all of Samsung’s process nodes.”

The pre-manufacturing flow in Closed-Loop DFM, called PRISM (Pattern Recognition & Identity Scoring Method), analyzes an IC design by deconstructing it into layout patterns and, using the Calibre Pattern Matching™ solution, identifying patterns known to have been yield detractors in the past. Samsung then uses Calibre LFD™ software along with other Calibre DFM products to spot previously unknown potential lithography hotspots and analyze their likely impacts on manufacturability. Samsung and the customer jointly make the best use of PRISM results to determine design and/or manufacturing changes needed to ensure that the customer’s unique design style achieves target yields and reduces production ramp variability.

After manufacturing, a second Closed-Loop DFM flow called FLARE (Failure anaLysis And yield Rank Estimation with DFM hotspot database) identifies yield-limiting layout patterns based on silicon results. Fail data from wafer test are diagnosed by the Foundry customer and analyzed by Samsung Foundry to identify unique layout patterns that cause yield loss. Samsung and its customers use this information to analyze systematic issues caused by physical design features to improve the ramp-up speed for design re-spins, as well as for new designs using the same IP blocks and or subsystems. Samsung Foundry also uses FLARE data to improve its DFM kits to share silicon findings with customer designers. FLARE uses the Tessent Diagnosis tool for layout-aware diagnosis, the Calibre Pattern Matching solution for generating a hotspot database, and statistical analysis in the Tessent YieldInsight® product to identify the yield limiting layout patterns.

The Closed-Loop DFM flows are in production use today for customers of Samsung Foundry services. While proven in 14 nm technology, the flows can be used for ICs manufactured with other Samsung process nodes.

At the 2016 Design Automation Conference, Mentor and Samsung are co-hosting a lunch seminar entitled “Accelerate Yield Ramps with Samsung Foundry Closed-Loop DFM and Mentor Tools.” The event is Monday, June 6, from 12:00 to 1:30 PM. Interested customers can https://www.mentor.com/products/ic_nanomete register for the event using this registration link r_design/events/samsung-dac-lunch-seminar

About Mentor Graphics

Mentor Graphics Corporation is a world leader in electronic hardware and software design solutions, providing products, consulting services and award-winning support for the world’s most successful electronic, semiconductor and systems companies. Established in 1981, the company reported revenues in the last fiscal year of approximately $1.18 billion. Corporate headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777. Web . http://www.mentor.com site: